FIG. 2

— PRIOR ART —

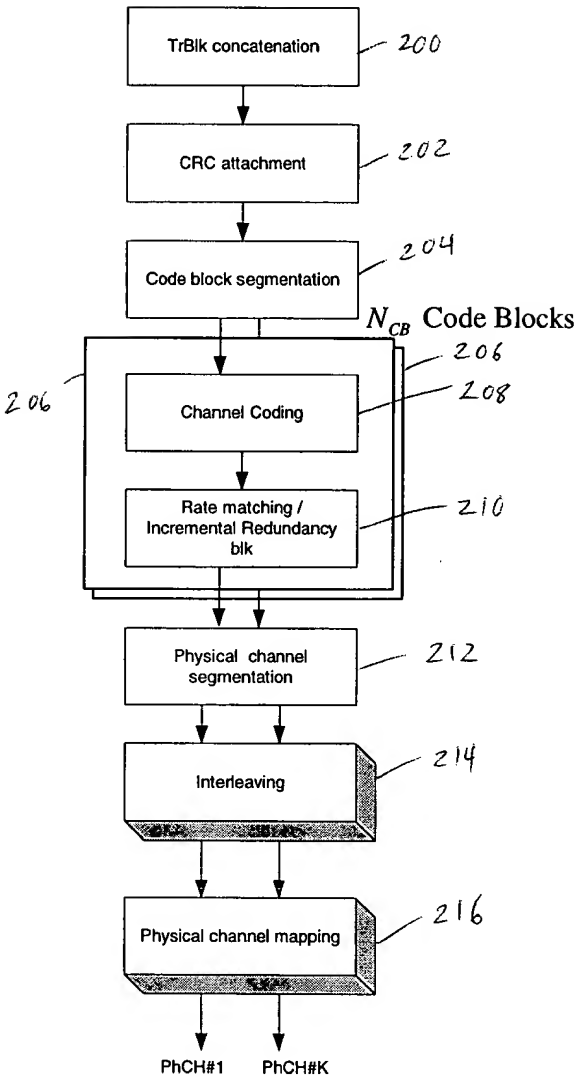
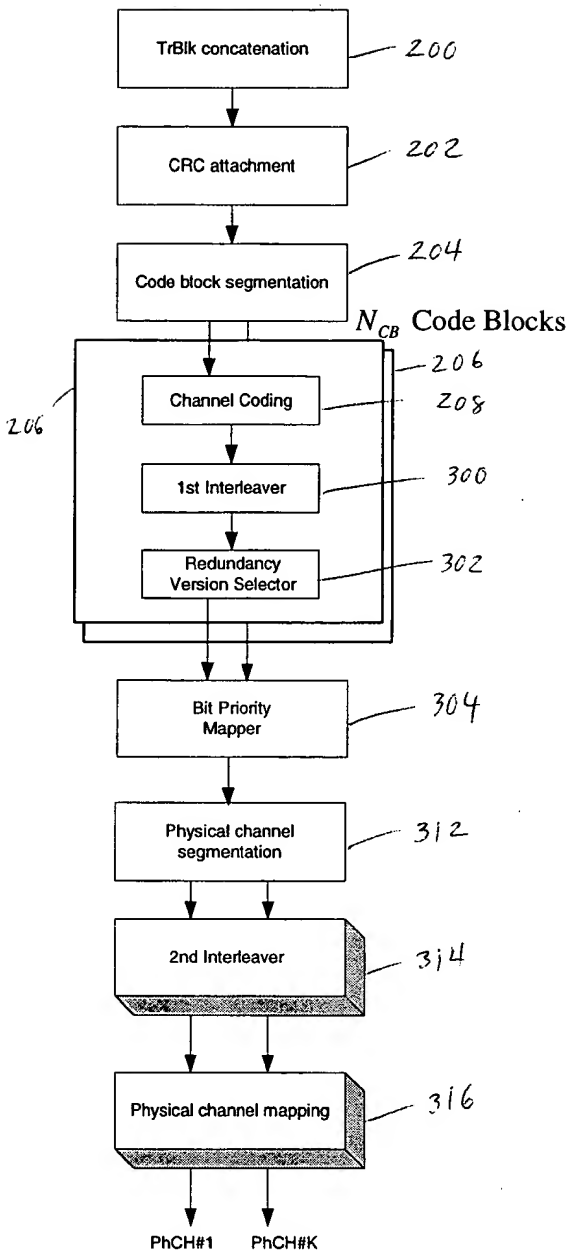


FIG. 3



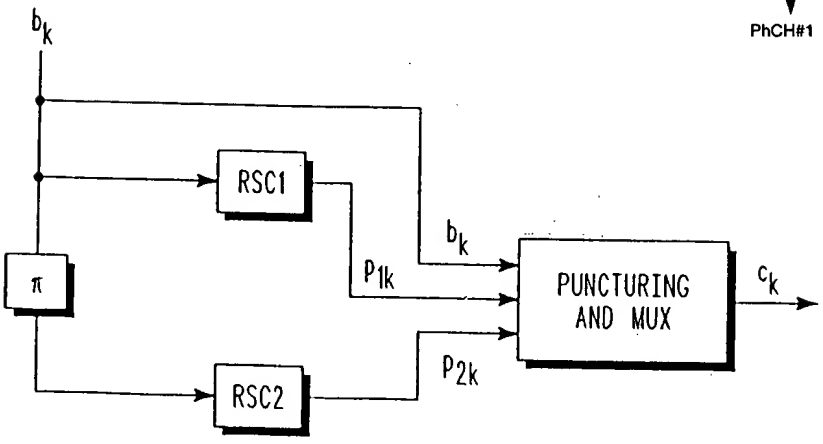


FIG. 1

— PRIOR ART —

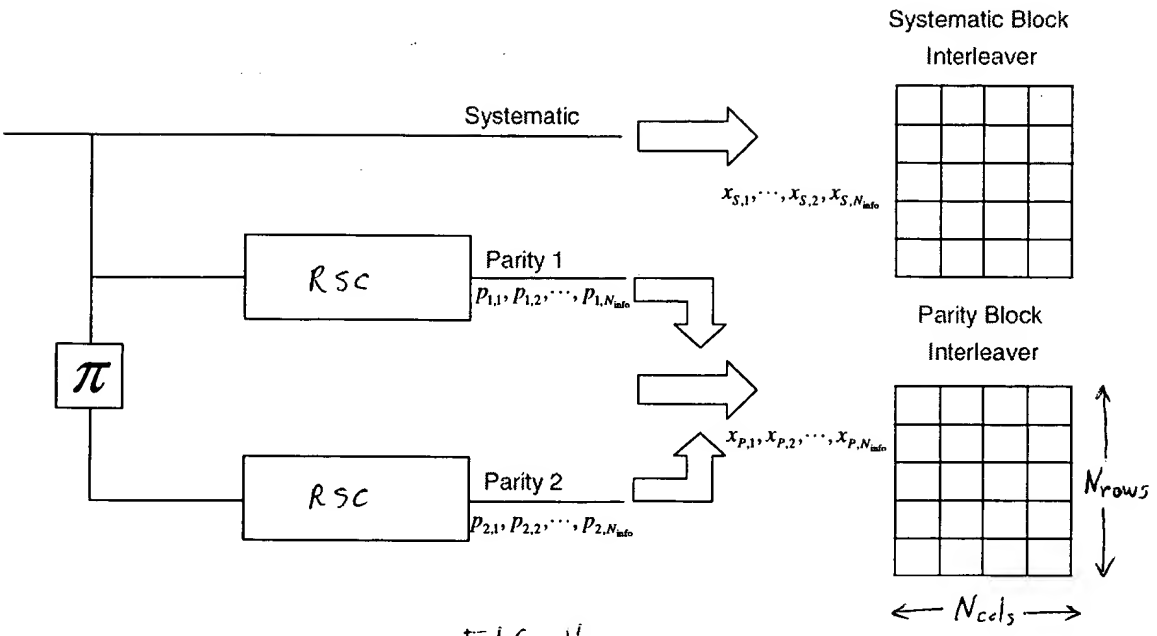

Systematic Block
Interleaver
Systematic
$x_{S,1}, \cdots, x_{S,2}, x_{S,N_{info}}$
RSC
Parity 1
$p_{1,1}, p_{1,2}, \cdots, p_{1,N_{info}}$
π
Parity Block
Interleaver
$x_{P,1}, x_{P,2}, \cdots, x_{P,N_{info}}$
RSC
Parity 2
$p_{2,1}, p_{2,2}, \cdots, p_{2,N_{info}}$
N_{rows}
N_{cols}

FIG. 4

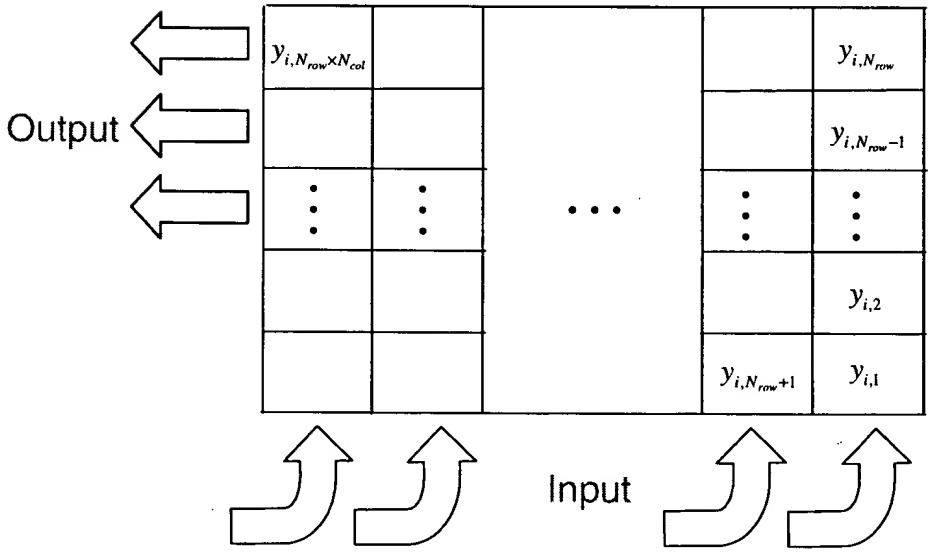

Output
$y_{i,N_{row} \times N_{col}}$
$y_{i,N_{row}}$
$y_{i,N_{row}-1}$
$y_{i,2}$
$y_{i,N_{row}+1}$
$y_{i,1}$
Input

FIG. 5

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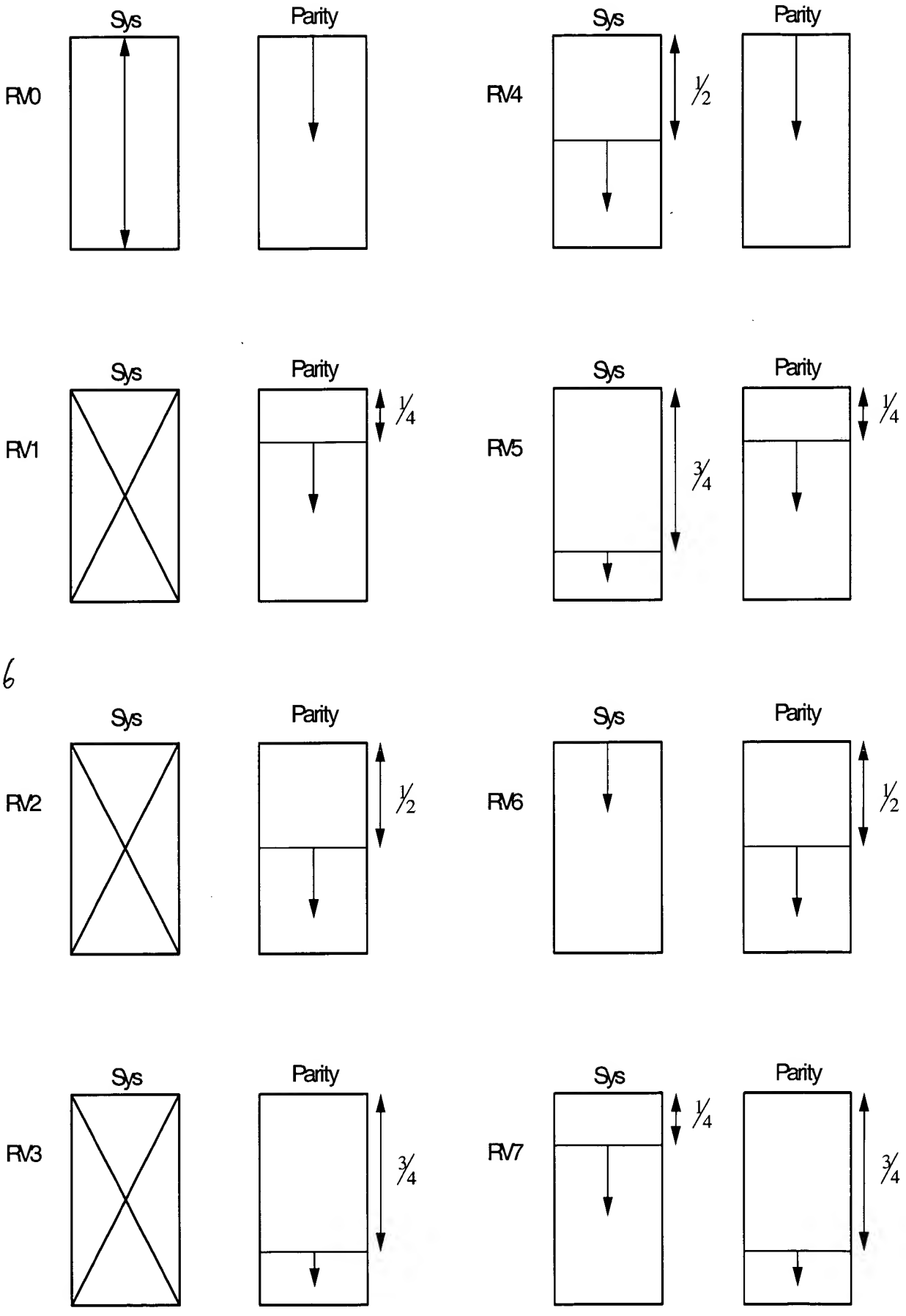

FIG. 6

09868274 - 050802

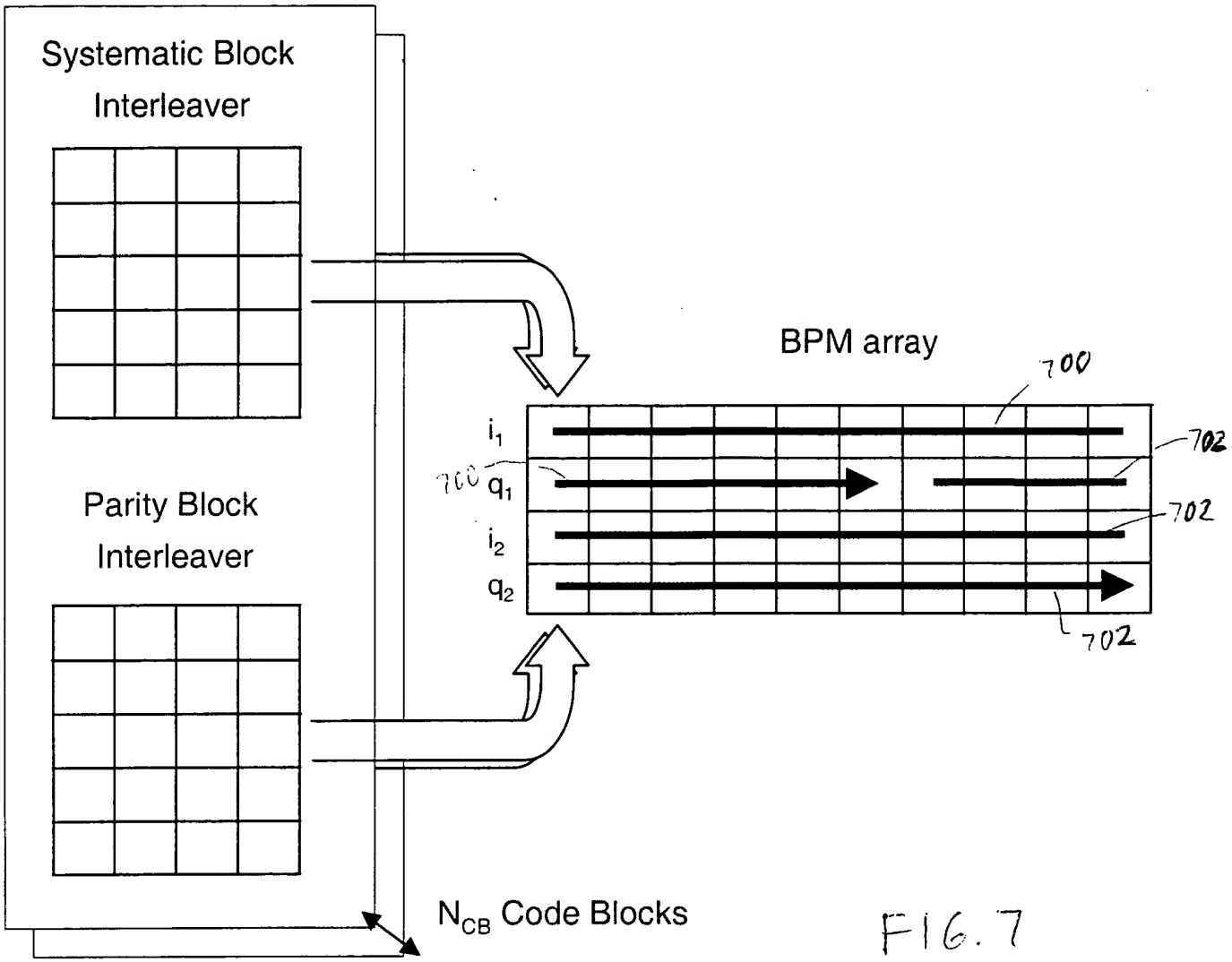

FIG. 7

09606544 - 062604

$$P_1 = \begin{bmatrix} 1 & 1 & 1 & 1 & 1 & 1 \\ 0 & 0 & 1 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 \end{bmatrix}, P_2 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 & 0 & 1 \end{bmatrix}, P_3 = \begin{bmatrix} 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 1 & 0 & 0 & 1 \\ 0 & 0 & 1 & 0 & 0 & 1 \\ 0 & 0 & 0 & 0 & 0 & 0 \\ 1 & 0 & 0 & 0 & 1 & 0 \\ 0 & 1 & 0 & 1 & 0 & 0 \end{bmatrix}$$

FIG. 8

09606241 - 040905

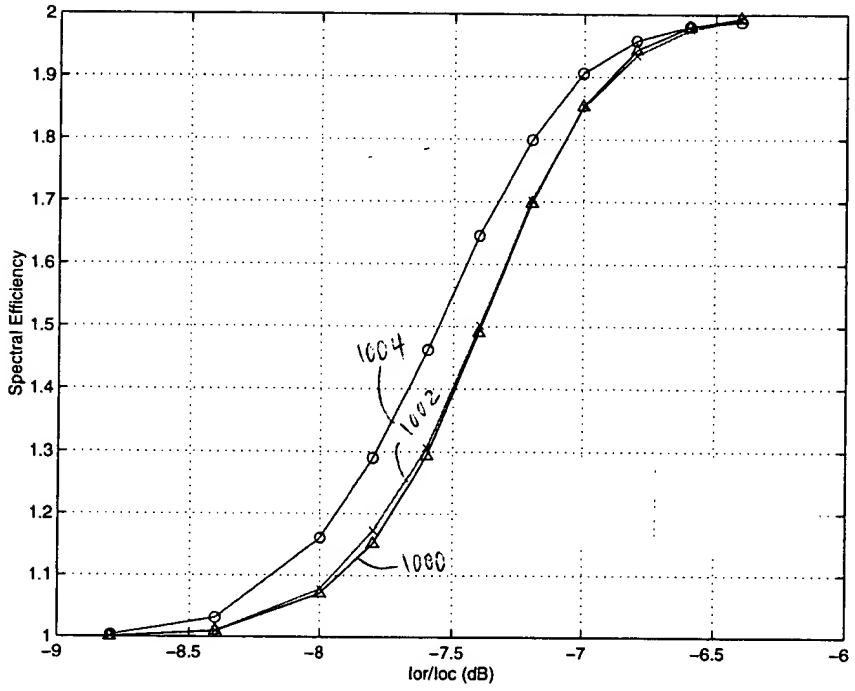

FIG. 9

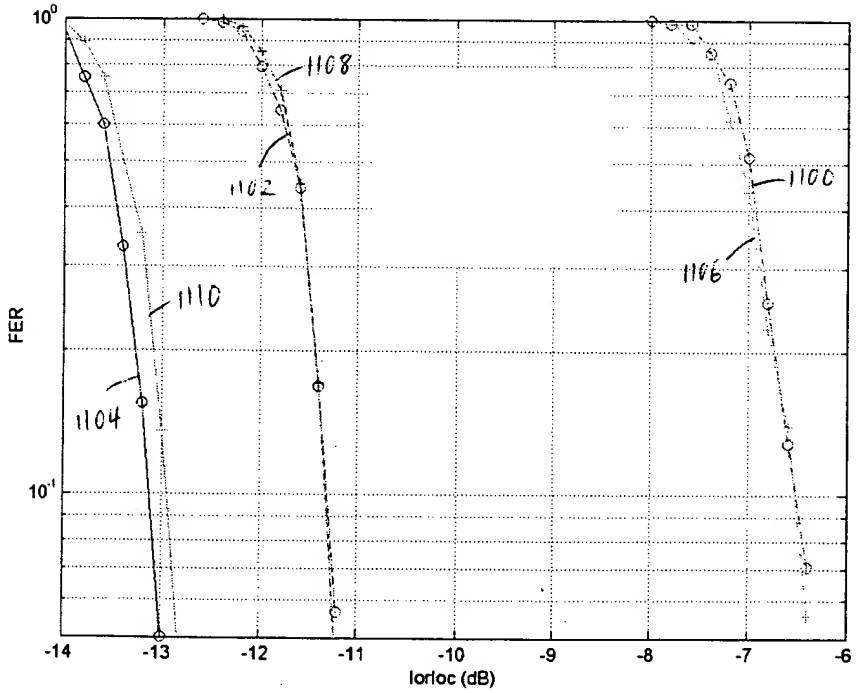

FIG. 10

Docket # 020168

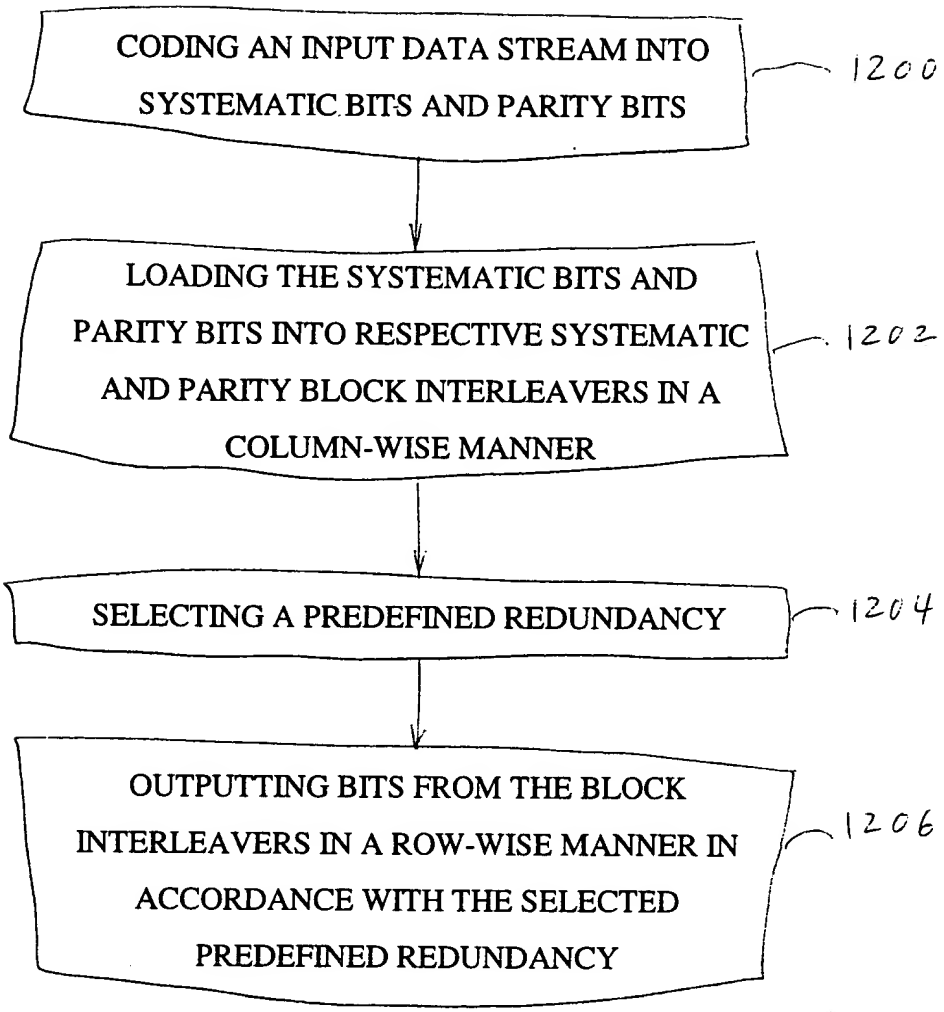

FIG. 11

Qualcomm Exhibit 1009